

The diagram illustrates a radio receiver system architecture. It features two antennas, ANT#1 and ANT#2, at the input. ANT#1 is connected to a first RF (Radio Frequency) block, labeled 1. ANT#2 is connected to a second RF block, labeled 2. Both RF blocks feed into a central SIGNAL PROCESSING UNIT, labeled 3. The SIGNAL PROCESSING UNIT is bidirectionally connected to a MAIN CONTROL UNIT, labeled 5. The MAIN CONTROL UNIT is responsible for converting reception levels into display formats and managing display timings. It is also bidirectionally connected to an INPUT UNIT, labeled 7, and a DISPLAY UNIT, labeled 6. The DISPLAY UNIT provides visual feedback, such as LED flickering or LCD character display of numerical values. The MAIN CONTROL UNIT outputs to a DEMODULATING UNIT, labeled 4, which produces the final BIT OUTPUT. Additionally, the MAIN CONTROL UNIT provides RECEPTION LEVEL 1 to the first RF block and RECEPTION LEVEL 2 to the second RF block.

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graph TD
    ANT1[ANT#1] --> RF1[1 RF]
    ANT2[ANT#2] --> RF2[2 RF]
    RF1 --> SPU[3 SIGNAL PROCESSING UNIT]
    RF2 --> SPU
    SPU <--> MCU[5 MAIN CONTROL UNIT  
(CONVERTS RECEPTION LEVELS OBTAINED  
FROM RFs TO CORRESPONDING DISPLAY FORMAT  
AND DISPLAY AT PRESCRIBED TIMINGS)]
    MCU <--> IU[7 INPUT UNIT]
    MCU <--> DU[6 DISPLAY UNIT  
• LED: DISPLAY BY FLICKERING OR COLOR  
• LCD: DISPLAY BY CHARACTERS AND  
NUMERICAL VALUES]
    MCU -- RECEPTION LEVEL 1 --> RF1
    MCU -- RECEPTION LEVEL 2 --> RF2
    SPU --> DU[4 DEMODULATING UNIT]
    DU --> BO[BIT OUTPUT]
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DISPLAY UNIT

- LED: DISPLAY BY FLICKERING OR COLOR
- LCD: DISPLAY BY CHARACTERS AND NUMERICAL VALUES

FIG. 2

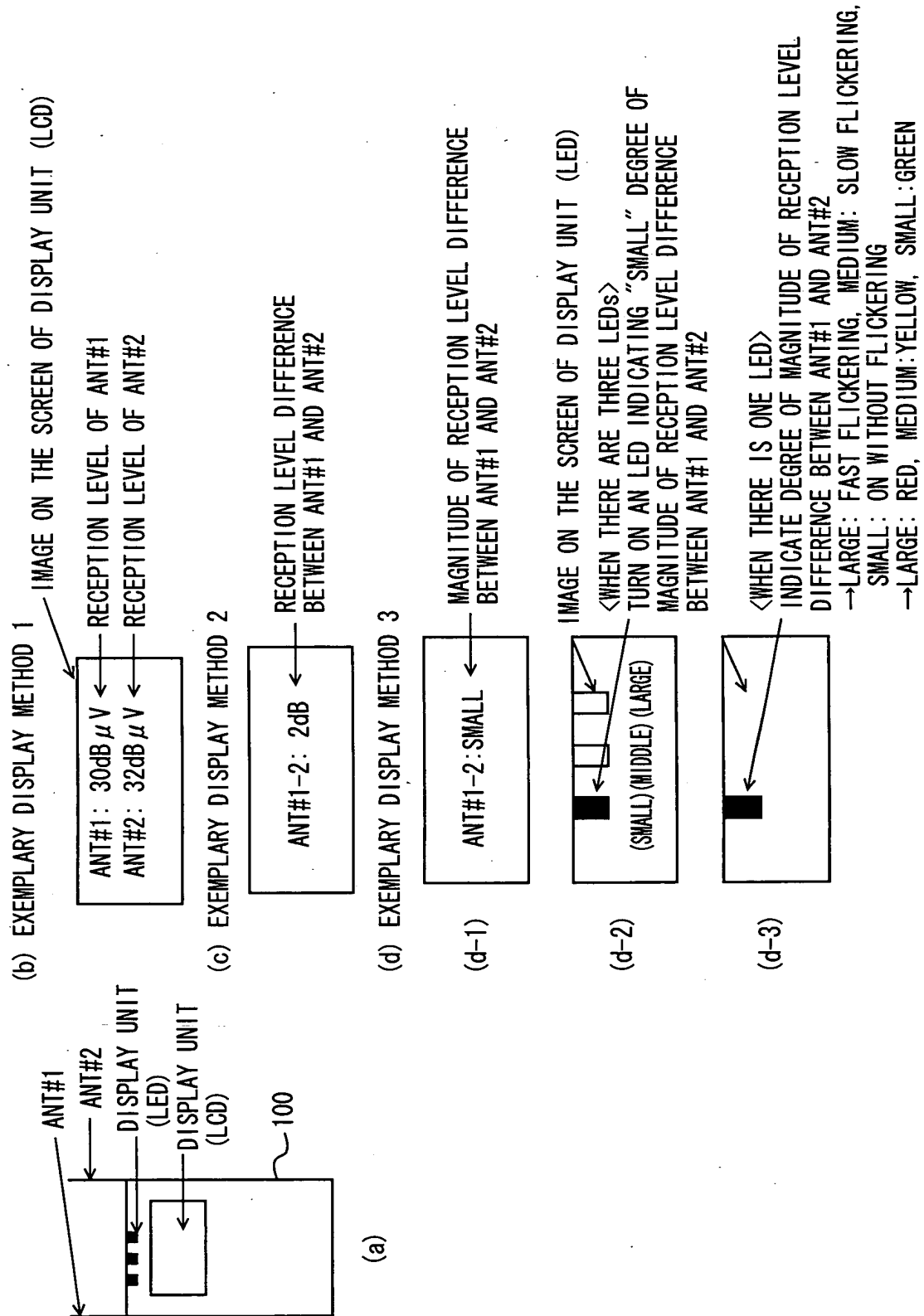


FIG. 3

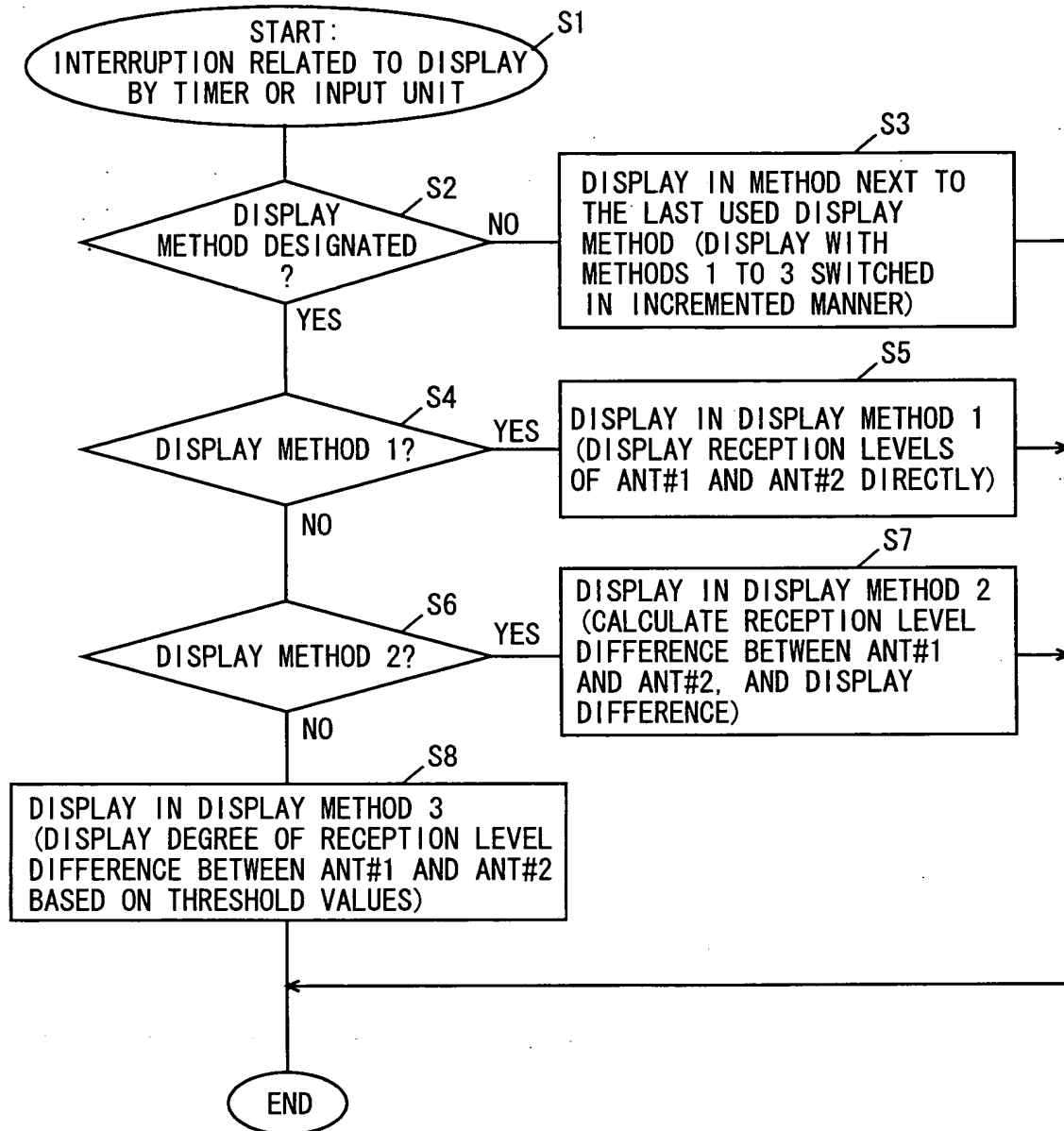


FIG. 4

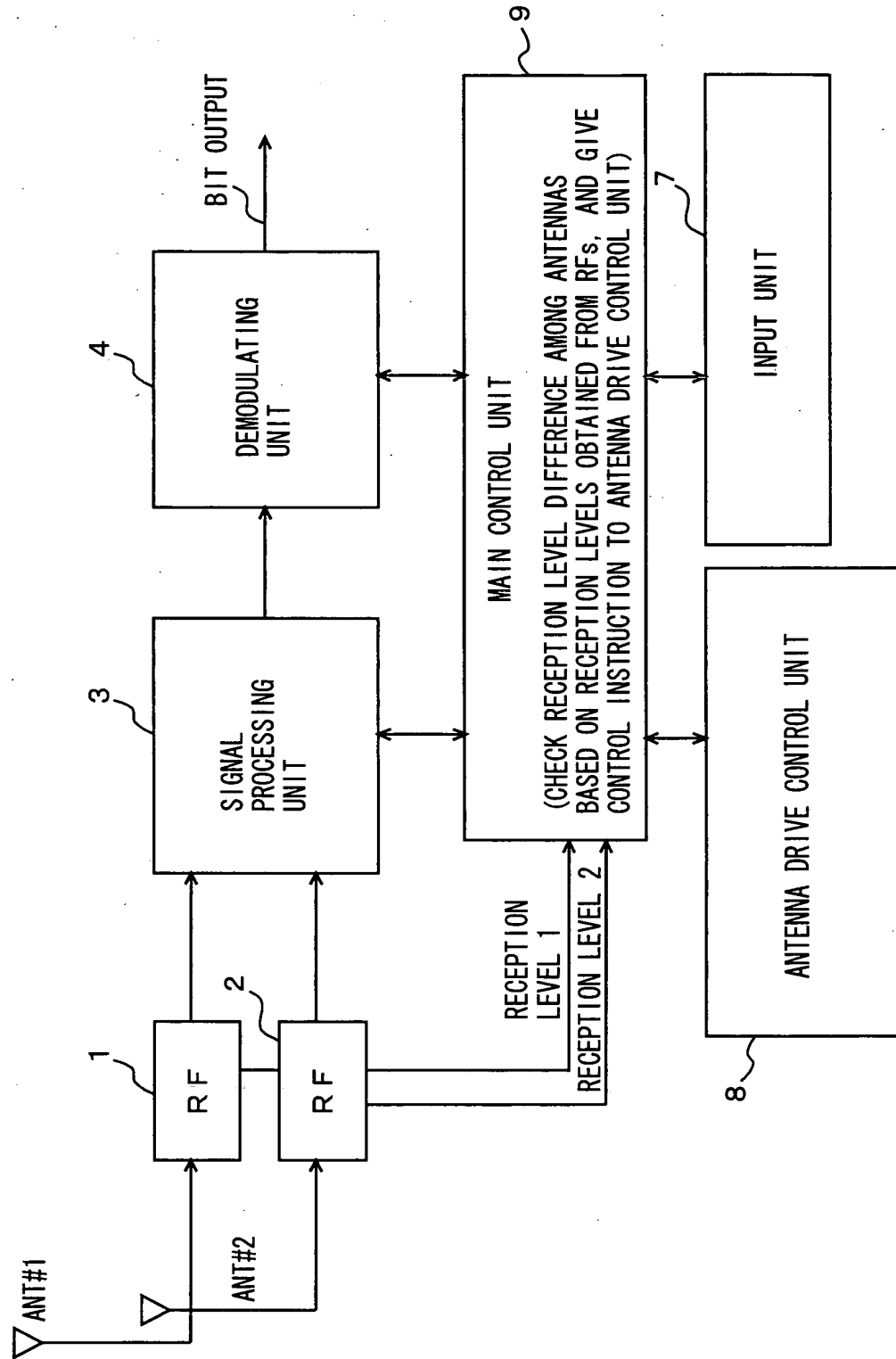


FIG. 5

